**SHRISHAIL DOLLE**
Master of Technology
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## Career Objective

I'm searching for a challenging position as a VLSI Physical Design Engineer. In order to develop high-performance circuits, I'll use my expertise in ASIC design flow, floorplanning, placement, routing, and timing analysis. In order to assist organizational growth and attain engineering excellence, I'm eager to innovate and optimize designs while also strengthening my abilities in modern technology.

## EDUCATION

- **Indraprasta Institute of Information Technology , Delhi** — *Aug,2025 - till date*
  *M.tech in Vlsi and Embedded systems* — CGPA: 9.43/100
- **Veermata Jijabai Technological Institute (VJTI) , Mumbai** — *2020-2024*
  *B.Tech in Electronics and Telecommunication* — CGPA: 8.25/10
- **Sangmeshwar College, Solapur** — *2017-2019*
  *HSC - Maharashtra State Board, Maharashtra* — Percentage: 78.31/100
- **Mangrule High School, Akkalkot** — *2011-2017*
  *SSC - Maharashtra State Board, Maharashtra* — Percentage: 93.40/100

## SKILLS and TECHNOLOGIES

- **Programming Languages :** Verilog , C++ , Python , TCL , Basic Linux.

P**roficient in Verilog, C++, Python, TCL, and Linux:** A versatile skill set enabling efficient design, verification, and automation of complex digital systems.

- **Strong foundation in digital design and verification:** Well-versed in industry-standard EDA tools and methodologies for creating reliable and high-performance digital circuits.
- **Technical Skills :** CMOS Technology , Digital Logic Design , ASIC Flow of VLSI , STA, RTL logic design,

**-Solid foundation in VLSI design:** Proficient in CMOS technology, digital logic design, and ASIC flow, including RTL design and static timing analysis.

**-Strong programming and algorithm skills:** Well-versed in C++, Python, and Verilog with an understanding of data structures and algorithms.

**-Interest in emerging technologies:** Keen on exploring the Internet of Things (IoT) and it's applications.

- **Tools :** Xillinx , PrimeTime , Fusion Compiler , Arduino.
- **Proficient in Xilinx design tools:** Skilled in using Xilinx's, Prime-Time and Fusion Compiler for designing and optimizing digital circuits.
- **Experienced with Arduino:** Hands-on experience in building and programming Arduino-based projects.
- **Strong foundation in digital design:** Solid understanding of digital logic and circuit design principles.

## CERTIFICATIONS

**–C++ for Beginners** covering topics from basic concepts to advanced techniques on Udemy.
**–Python from A-Z** Comprehensive C++ course on Udemy, covering fundamentals and OOPS.
**–Introduction and Programming with IoT Boards** Platform Coursera

## PROJECTS

· **MSI Protocol Implementation** *Aug-Dec 2025*

This project implements a **two-processor multi-level cache hierarchy** using the **MSI coherence protocol** and a snooping-based bus to maintain data consistency. It features a unique **write-through policy** for the L1 caches, ensuring that any modifications are immediately propagated to the shared L2 cache and main memory.The architecture is designed with **2-way set associative** caches at both levels and includes a dedicated bus arbiter to manage inter-processor communication. Through detailed Verilog simulation, the project verifies complex cache state transitions—such as the **I→M (Invalid to Modified)** transition—and validates the timing requirements of high-latency main memory access.

· **TSPC Multibit flip-flop Design** *Aug-Dec 2025*

This project explores the design and implementation of a **Multibit TSPC Flip-Flop** using a 65nm CMOS process to achieve high-speed, energy-efficient data storage. By utilizing a **True Single Phase Clock** architecture, the design minimizes clock skew and power consumption compared to traditional master-slave configurations.The workflow spans the entire VLSI design cycle, from **schematic capture and pre-layout simulation** to physical layout and extraction. The final phase involves rigorous **timing characterization and post-layout verification** to ensure performance reliability in modern high-density digital systems

· **Smart Toll System RTL to GDS Flow** *Aug-Dec 2025*

This project implements an automated **Smart Toll System** through a complete VLSI design cycle, transforming high-level Verilog RTL into a finalized GDSII layout. The design features integrated sensors and communication modules to manage vehicle detection and payment processing efficiently at the edge.The workflow covers critical stages including **Logic Synthesis**, floorplanning, and **Place and Route (PnR)** using a standard cell library to optimize area and power. Final verification involves **Static Timing Analysis (STA)** and Physical Verification (DRC/LVS) to ensure the hardware is fabrication-ready for modern ITS (Intelligent Transportation Systems) applications.

## Positions of Responsibility

**–Chief Execution Officer,** Rangawardhan , Marathi Cultural Club of VJTI *August,2022 - February,2023.*
CEO, Rangawardhan, VJTI's Marathi Cultural Club. Led and managed the core team, overseeing various cultural events and initiatives. Fostered a vibrant community of Marathi enthusiasts at VJTI.

**–Member,** Society of Robotics and Automation, VJTI *Jun, 2021 - March,2022*
Active member of the Society of Robotics and Automation at VJTI. Contributed to team projects, workshops, and robotics competitions, fostering a passion for automation and robotics.

**–Cadet ,**9 Maharashtra Battalion (Mah Bn) NCC, Solapur *Jun 2014 - March,2016*
Dedicated NCC cadet at 9 Maharashtra Battalion, Solapur. Participated in various training camps, parades, and social service activities, honing leadership skills and discipline

## Achievements

**–MHT-CET** Scored 99.30 percentiles in Common Entrance Exam of Maharashtra *December 2020*
**–JEE Mains** Scored 94th percentile in JEE Main 2023 *February 2020*
**–JEE Advance** qualifying for JEE Advanced and ranking among India's top 10,000 students. *Oct 2020*
Awarded a 94th percentile in the JEE Main 2023. Qualified for the JEE Advanced and secured a rank among India's top 10,000 students, demonstrating exceptional engineering aptitude.
**–NCC** Achieved Grade "A" in the A Certificate NCC examination. *April 2017*

## Declaration

I hereby declare that all the information provided in this document is true to the best of my knowledge and belief.
**Shrishail Dolle**